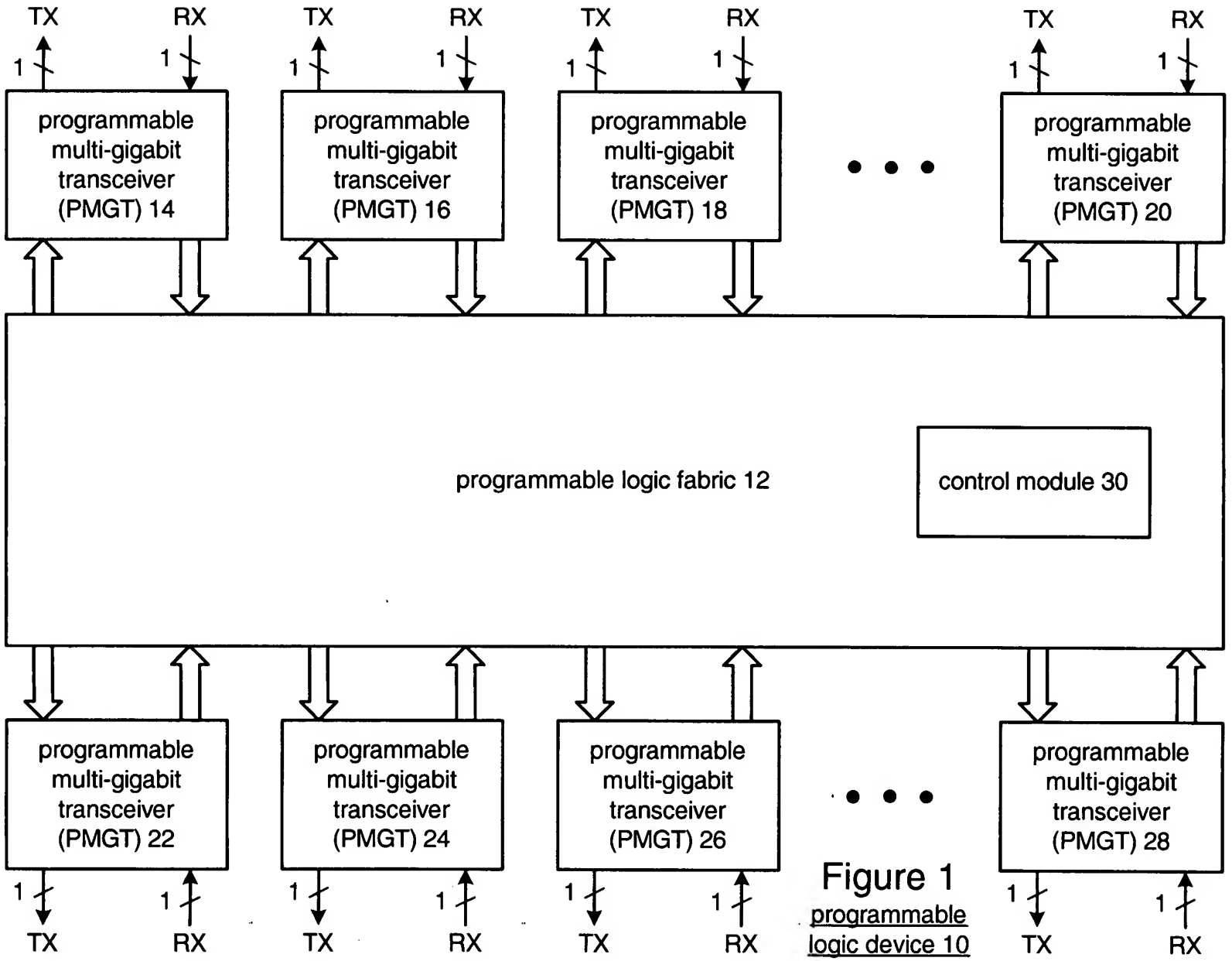

Figure 1
programmable logic device 10

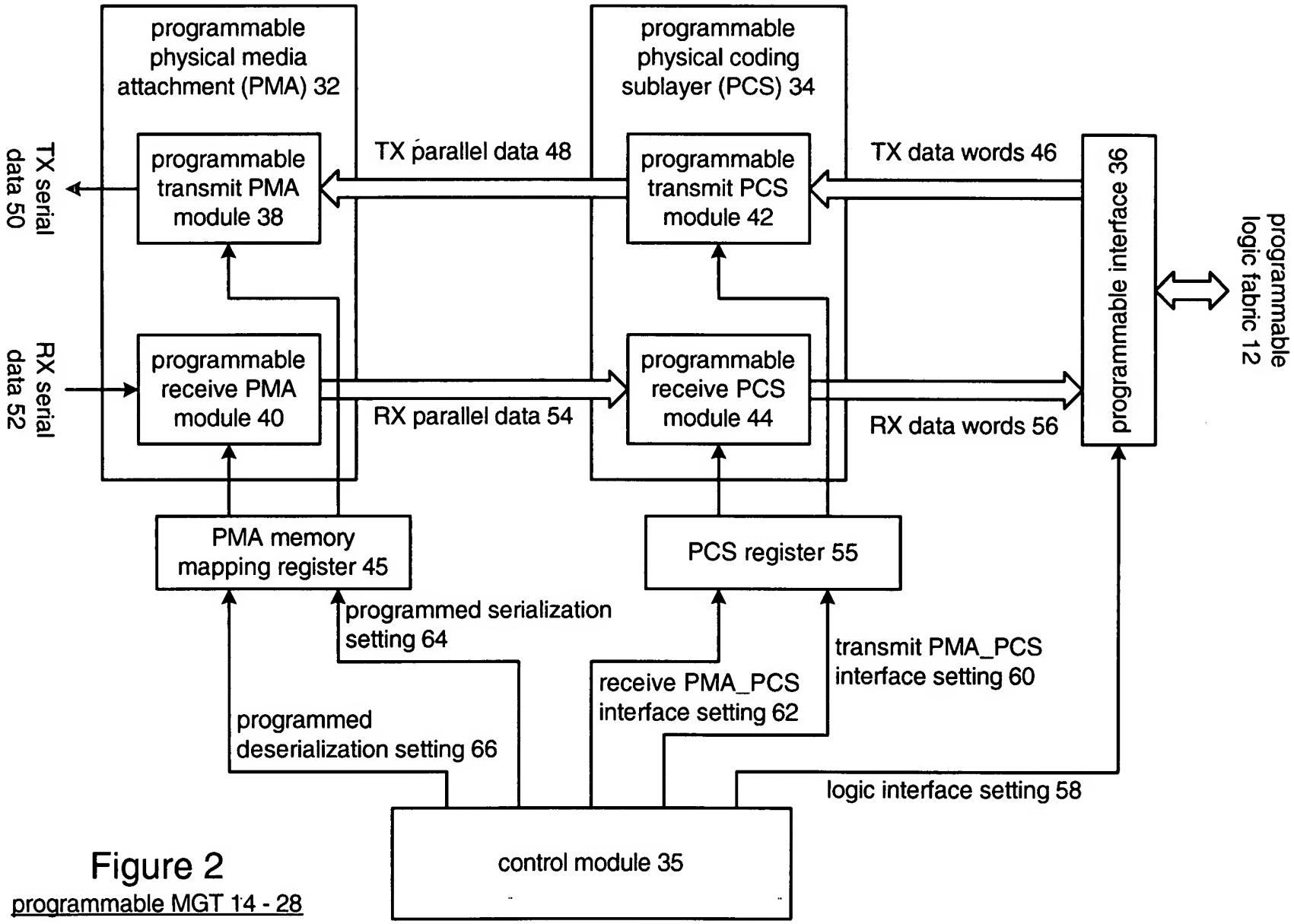

Figure 2

programmable MGT 14 - 28

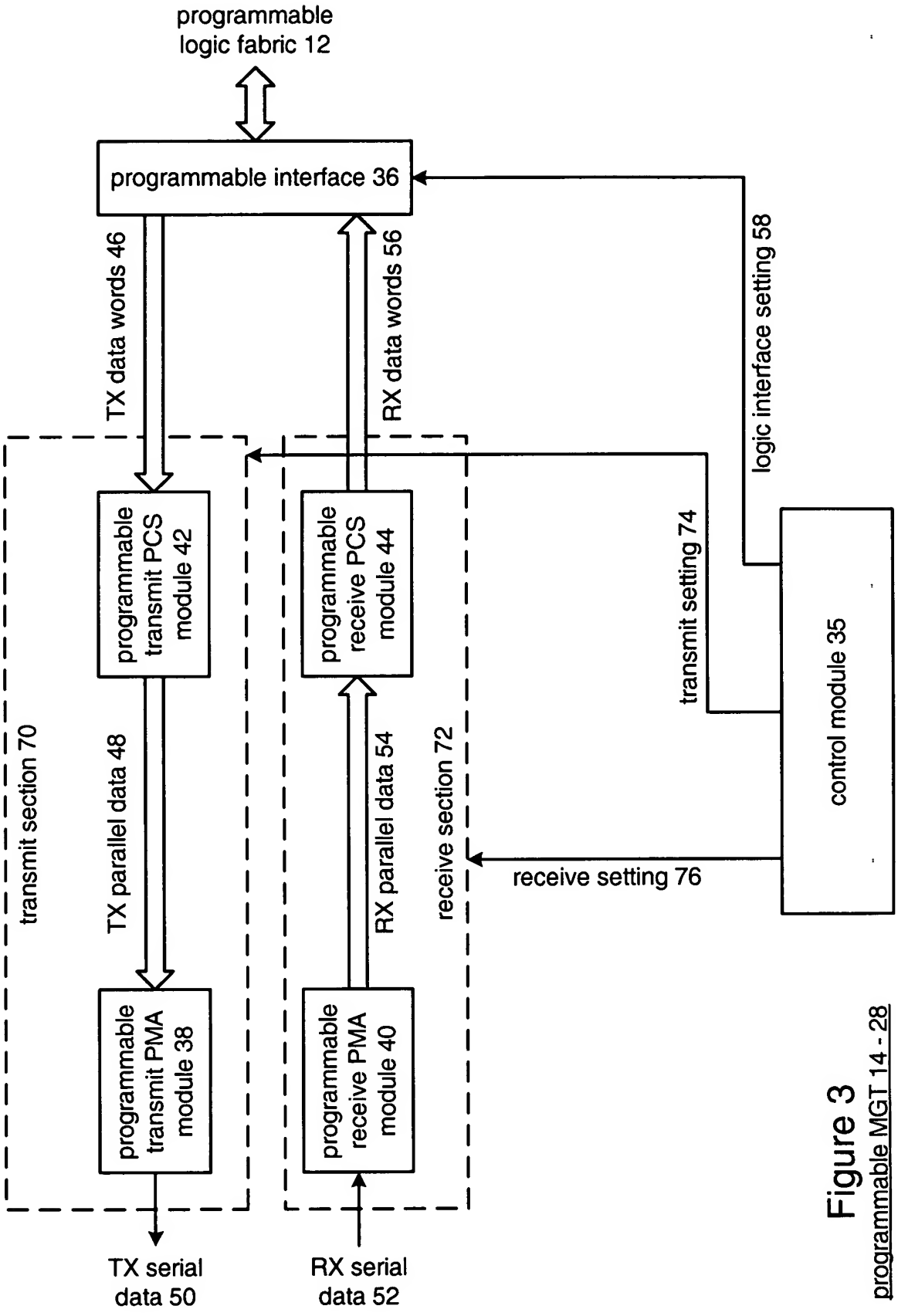

Figure 3
programmable MGT 14 - 28

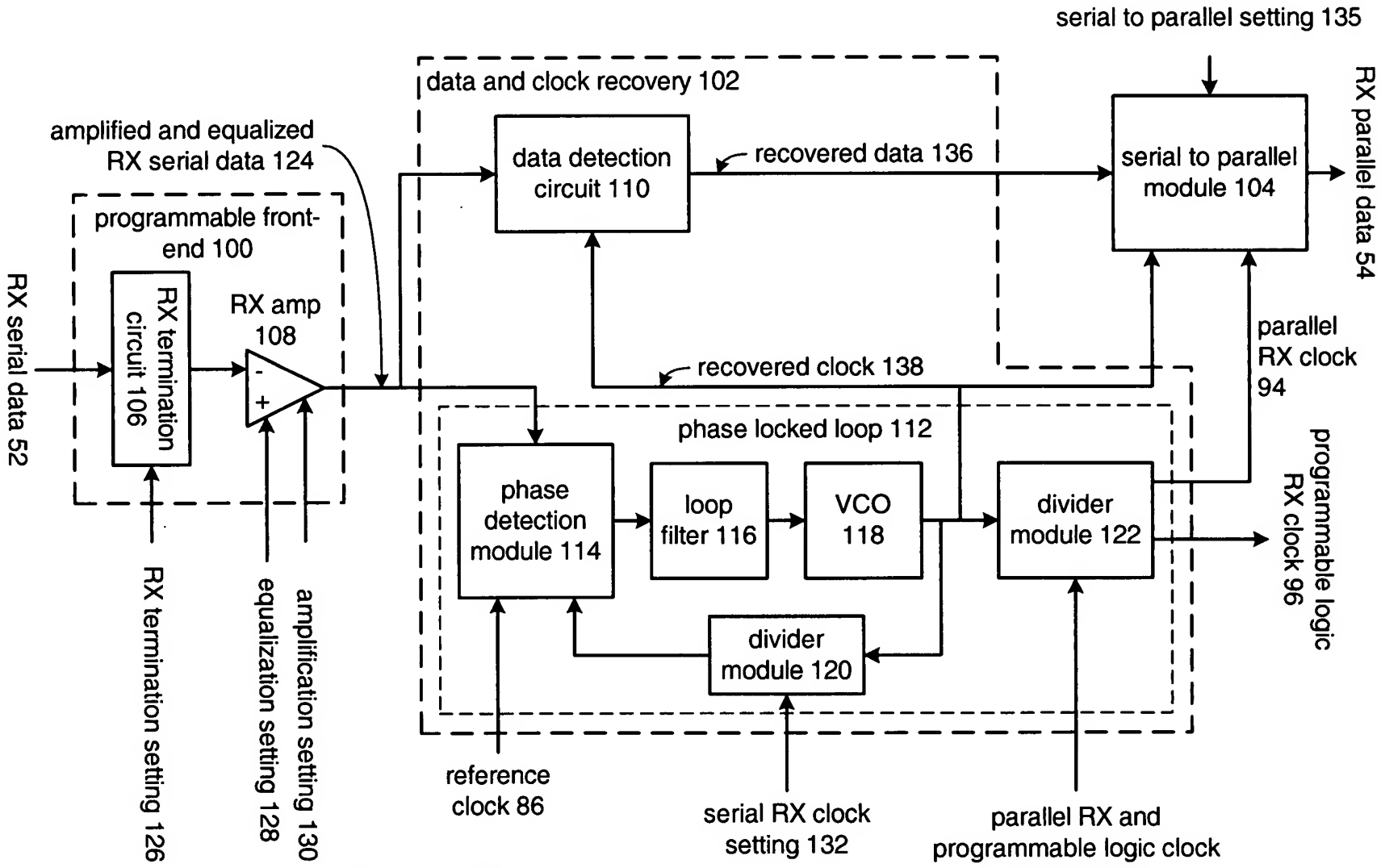

Figure 4A

programmable receive PMA module 40

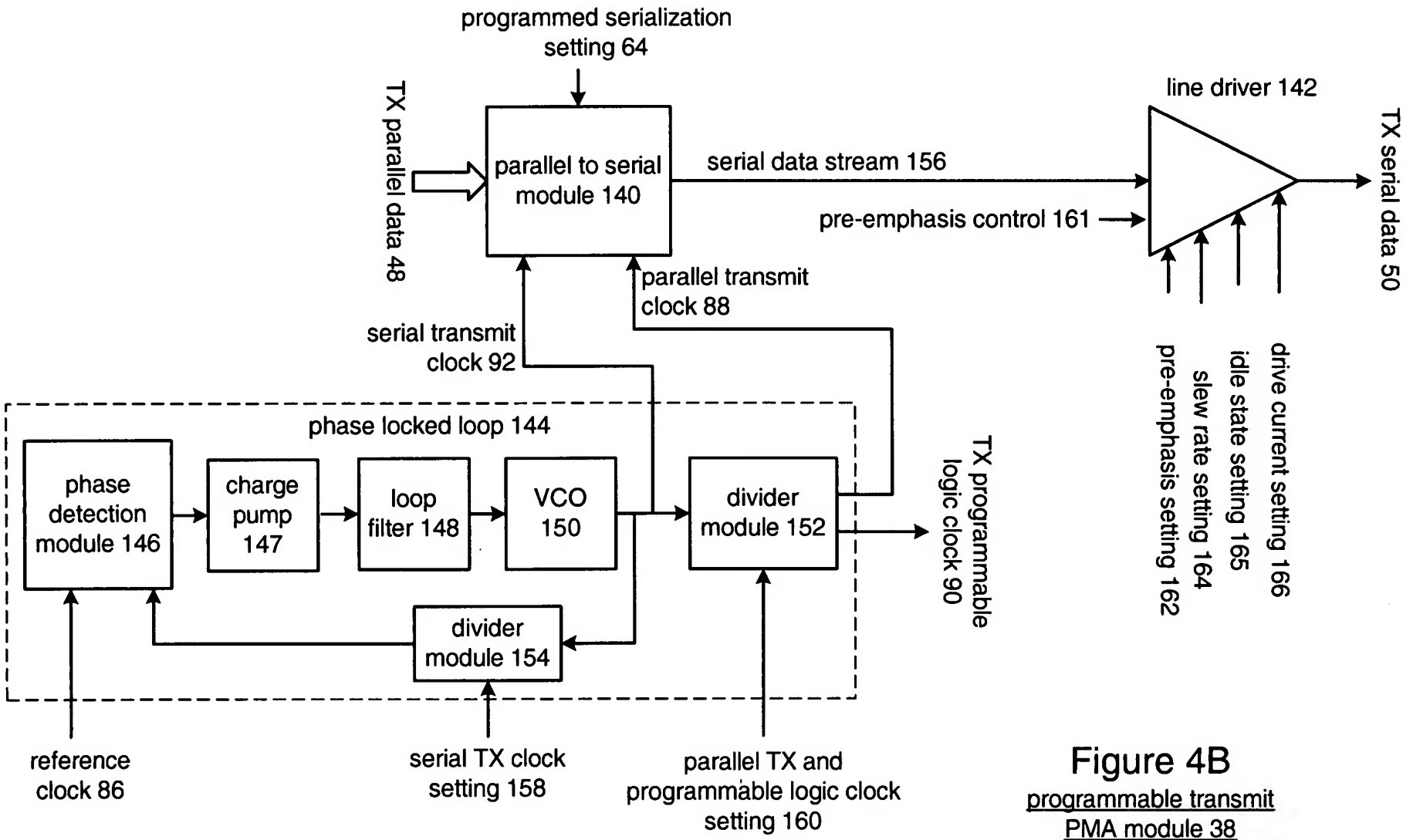

Figure 4B
programmable transmit PMA module 38

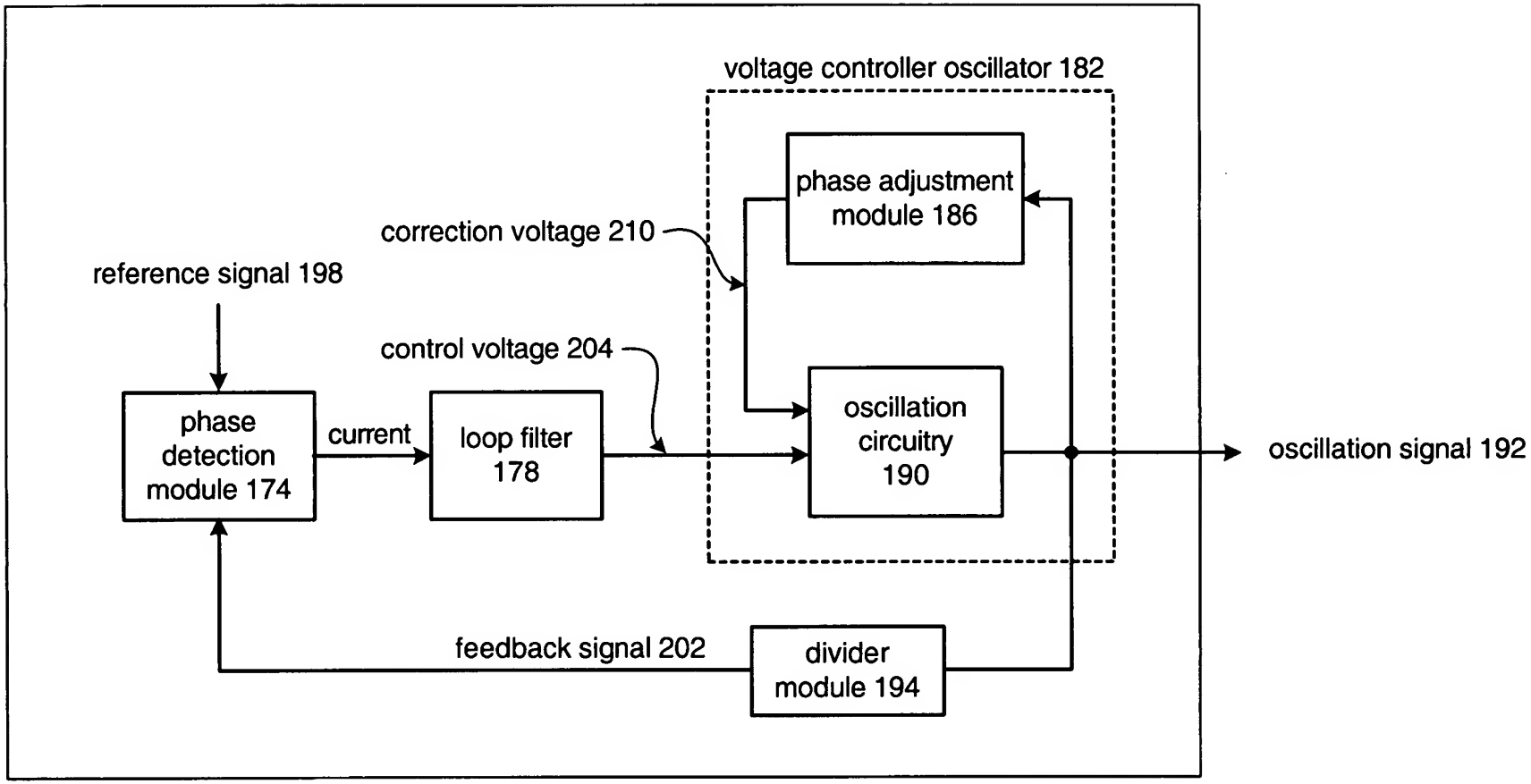

Figure 5

phase-locked loop 170

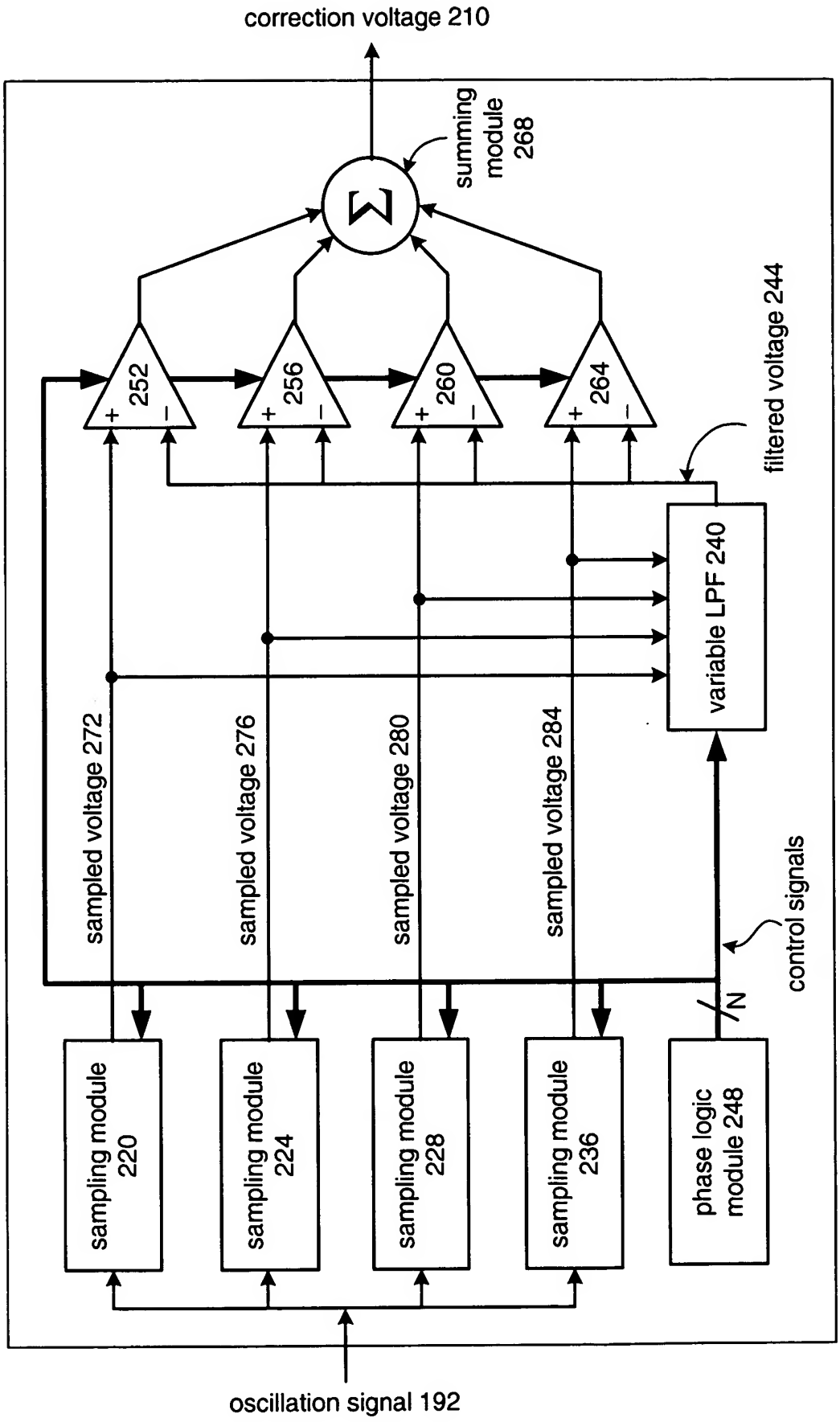

Figure 6

Phase adjustment module 186

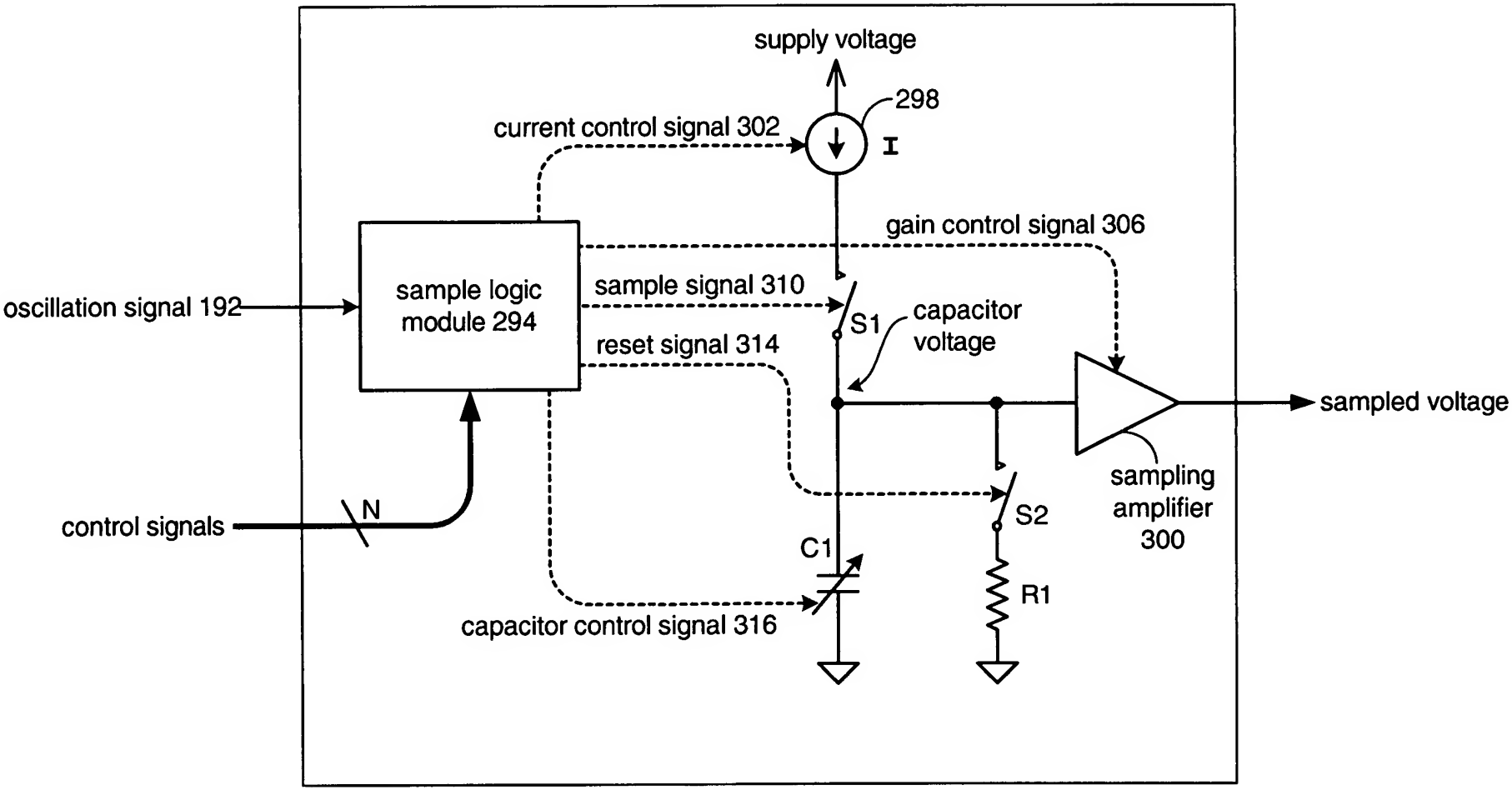

Figure 7

sampling module 290

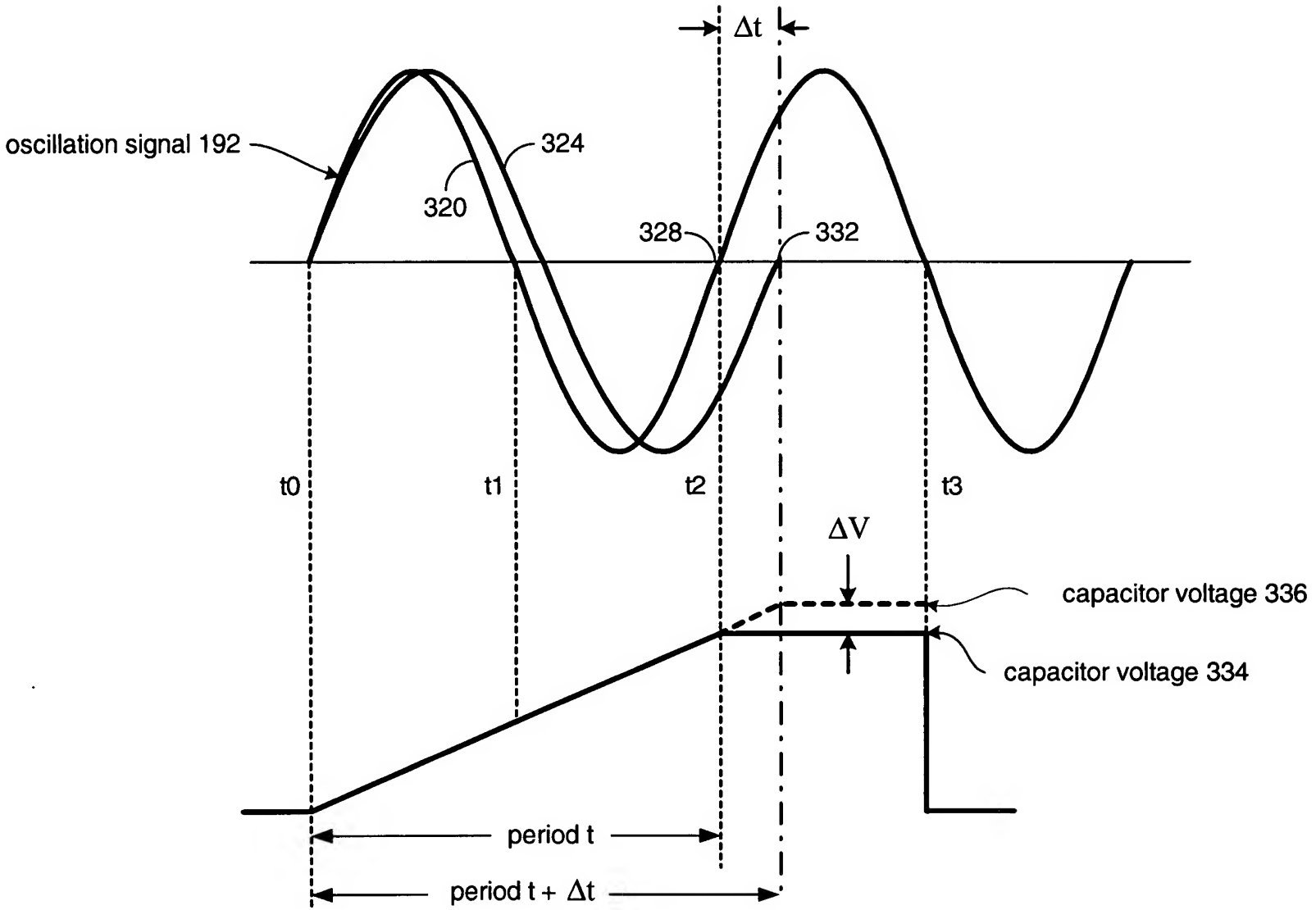

Figure 8

oscillation signal sampling

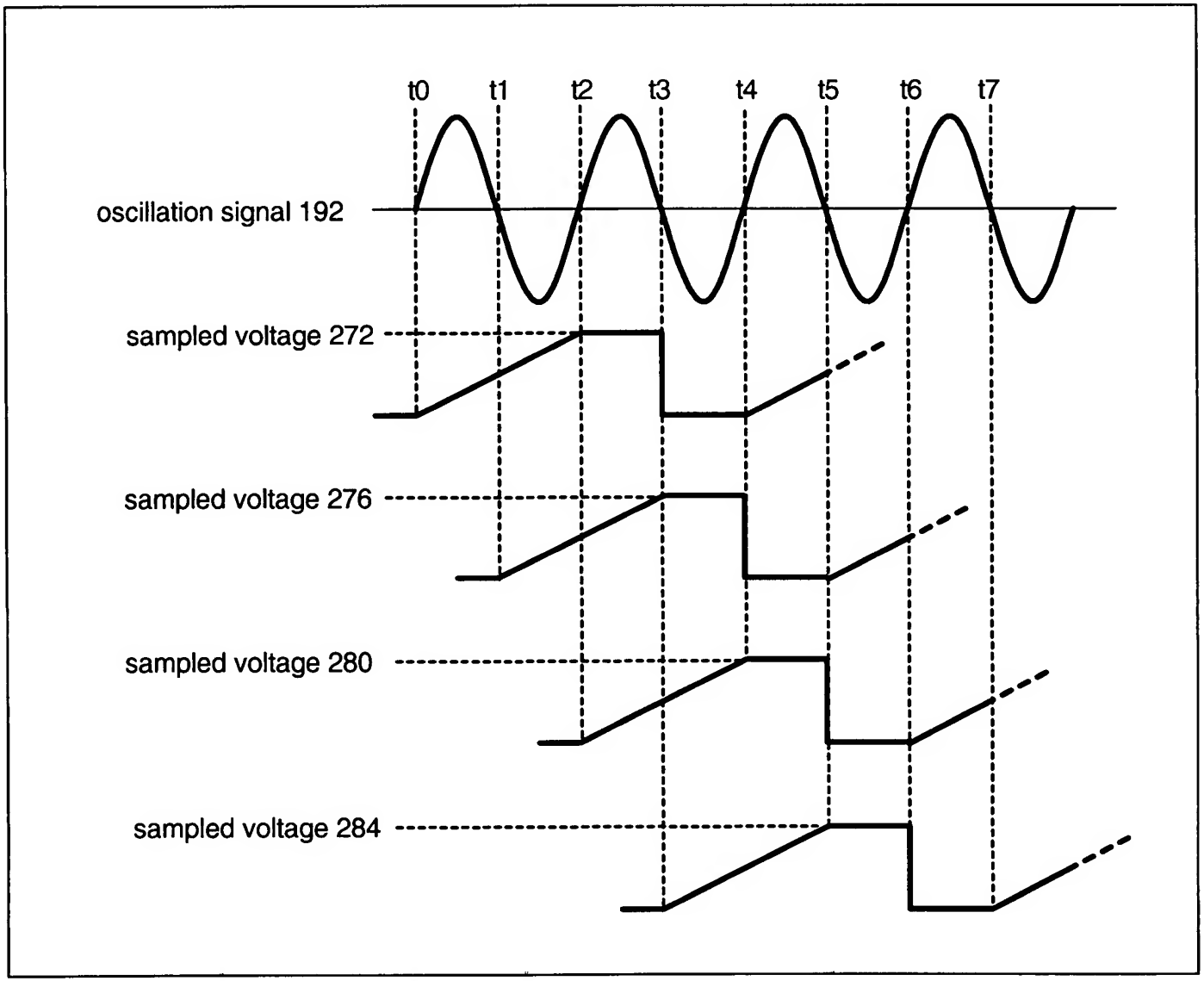

Figure 9
zero crossing sampling

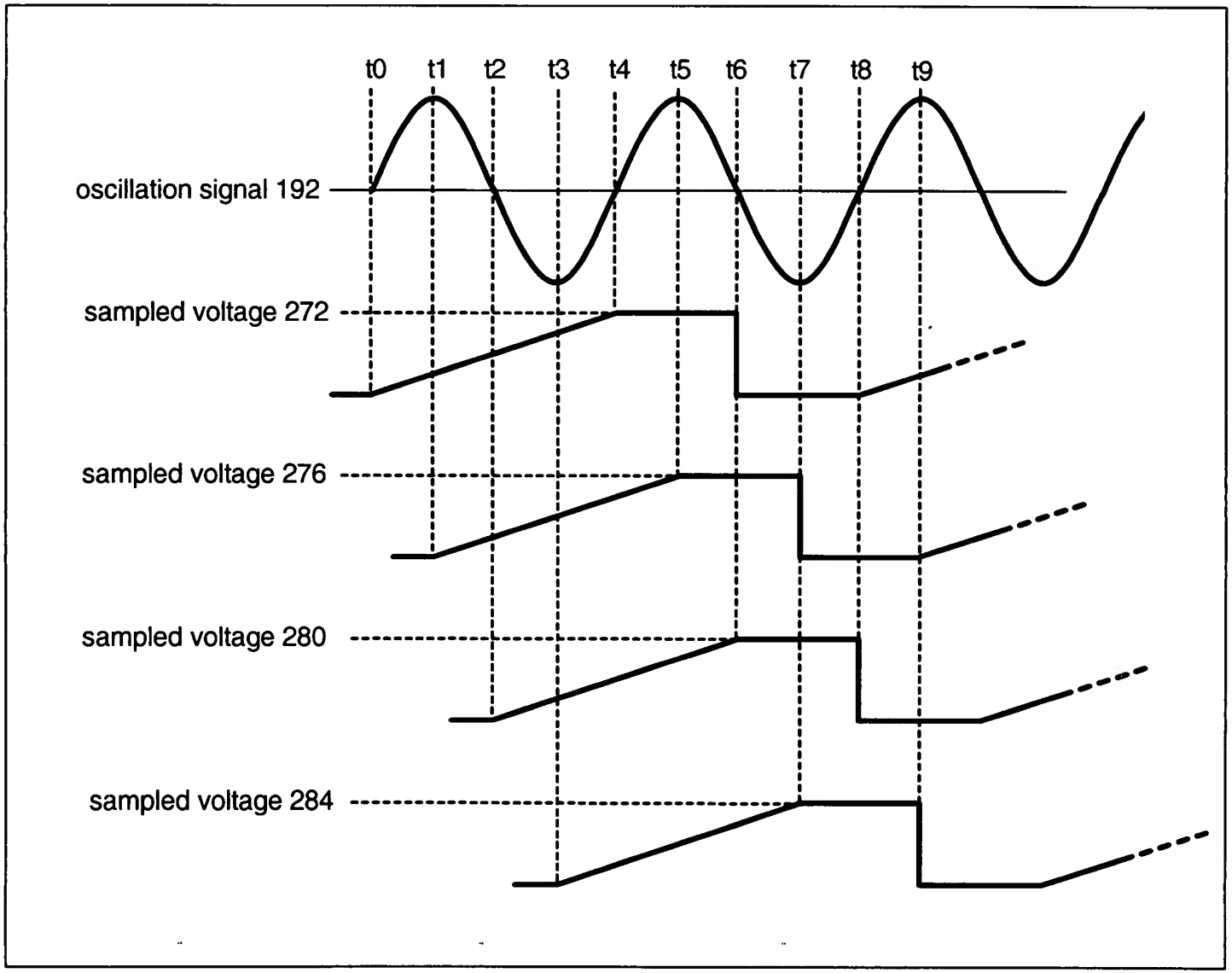

Figure 10
1/4 cycle sampling

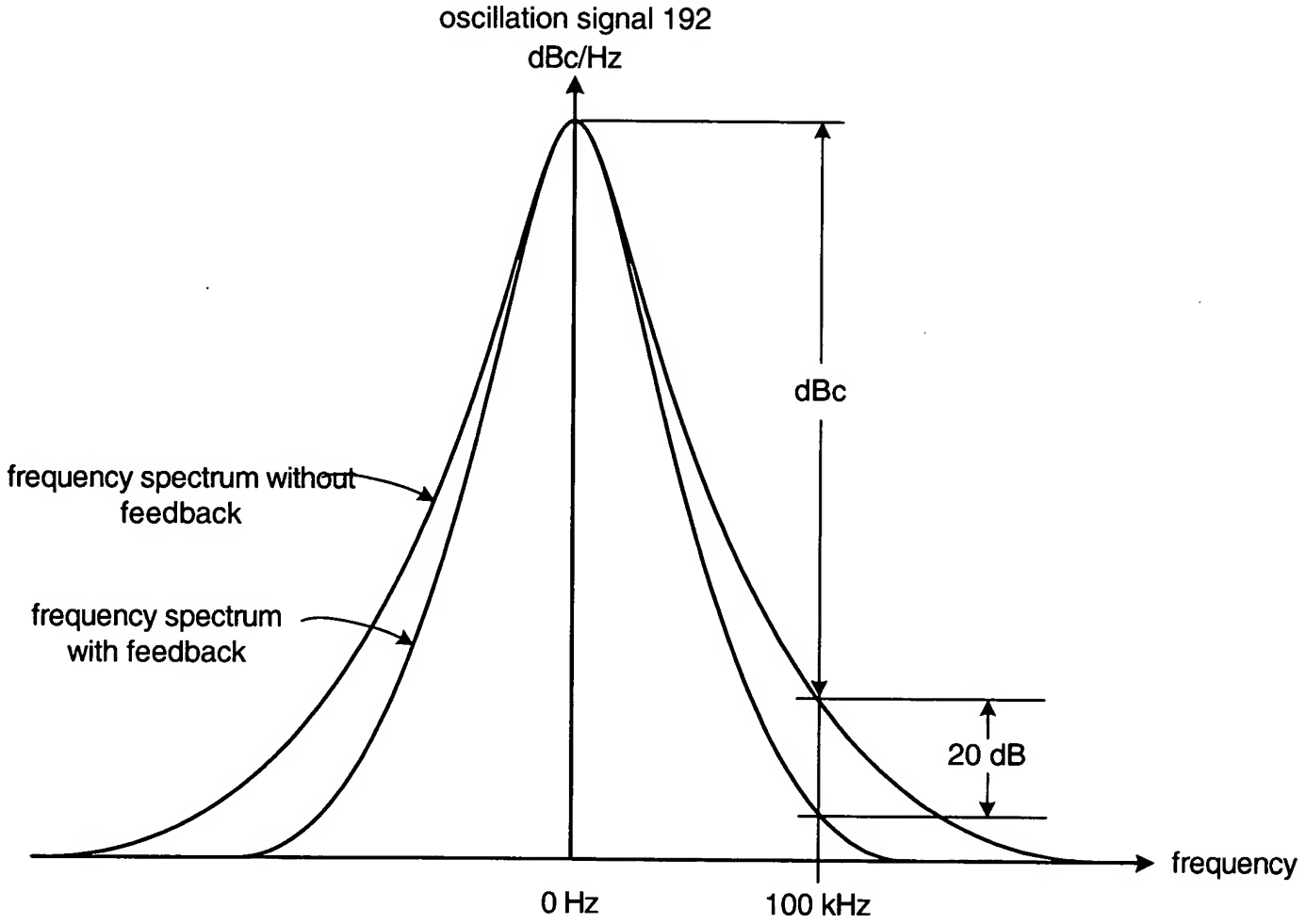

Figure 11

frequency domain phase noise plot

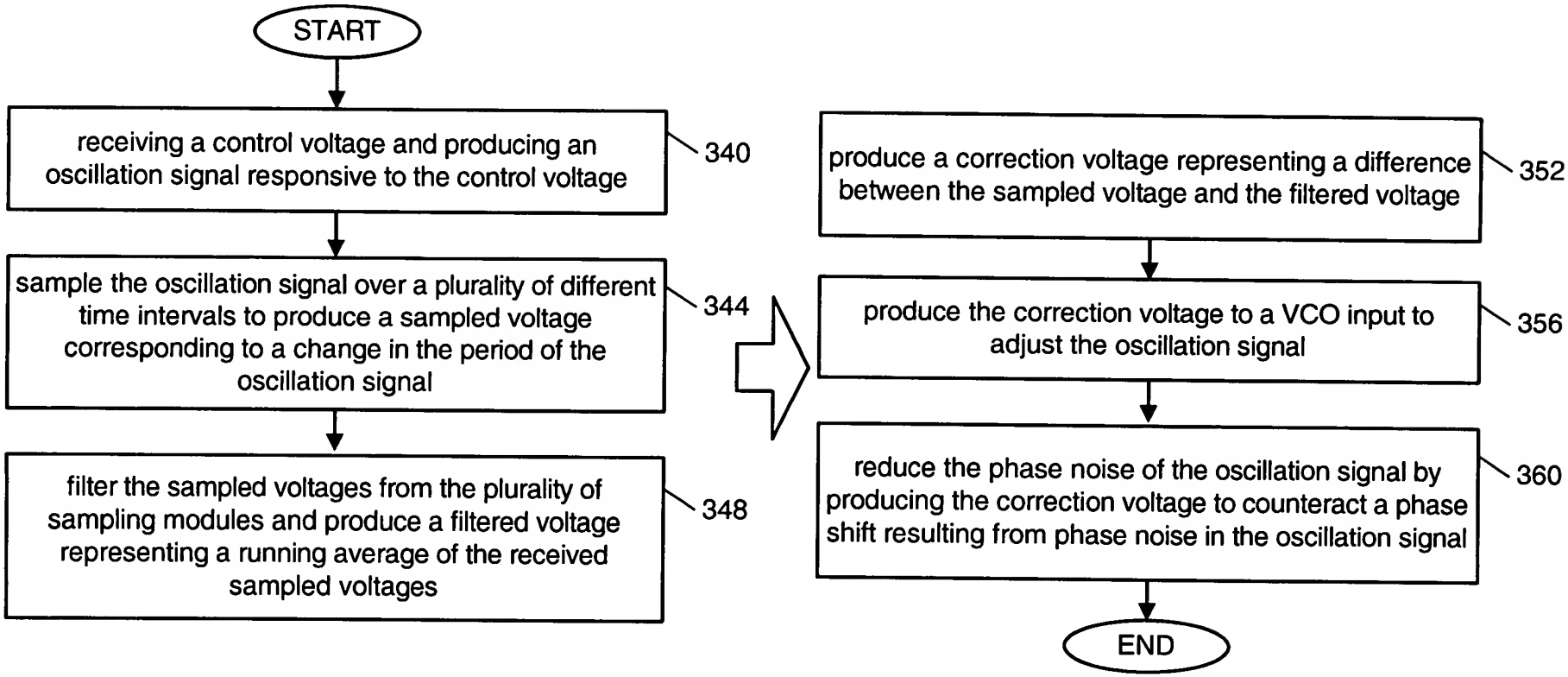

Figure 12
sampling method